

## Skills

- ✓ **Cloud System Architecture (5 years)**
  - Layered, event-driven, micro-services architectures for highly available systems; architecture&design patterns; requirements analysis
  - Automated delivery of scalable services with cost/resource optimization, versioned APIs and IoT friendly protocols
- ✓ **Technical Teams & Projects Management (12 year)**
  - Leadership and motivation of technical teams, overseeing projects, releases and customer accounts
  - Hiring, performance appraisals, tasks tracking, planning, milestones and progress reporting
- ✓ **Complex Telecommunication Electronic Systems Design (15 years)**
  - Architecture of electronic DSP-based cards and SoC with hardware accelerators and embedded real-time software
  - Production of Specification, functional requirements, firmware/software interface documents; architecture, sequence graphs

## Diplomas

- ✓ **Engineer Degree**, SUPAERO (Toulouse 1998-2001) : *Telecommunications, Electronics and Real Time Embedded Software*
- ✓ **Master in Micro-electronics Circuits and Micro-systems Design**, SUPAERO / Paul Sabatier University (Toulouse 2000-2001)

## Development tools

**Methodologies :** AGILE, UML, DDD, V-Model, System analysis, architecture&design patterns, SW components design for maximal reuse  
**Languages :** Python (expert), C/C++ (expert), Java, TypeScript, Groovy, Unix Shells, Matlab, Pascal, VHDL, HTML, Maple, TeX/LaTeX  
**Virtualization :** Docker (expert), Kubernetes, HA-Proxy, KVM, chroot, schroot  
**Frameworks :** FastAPI (expert), SpringBoot, Angular; SQLAlchemy/PostgreSQL, JPA/Hibernate, liquibase; NumPy, SciPy, Pandas  
**Technologies :** GPS/GNSS, LTE, IEEE802.16e (WIMAX), TCP/IP, UDP, CoAP, HTTP, HTTPS, PNG, JPEG, MPEG, BT601, BT656, ...  
**Environments :** Dia, Draw.io, MS-Visio, IntelliJ, Eclipse, Spyder, Jupiter, gVim, TI CCS, Lazarus, Glade, QtDesigner, Delphi, Visual C++  
**Version Control :** GIT (expert), GitHub, GitLab, Jira, BitBucket, Android//repo, SVN, BZR, ClearCase, CVS, Collabnet  
**CPU/DSP/μC cores :** Cadence Fusion, Verisilicon ZSP5x0, Synopsys Arc, NXP CoolFlux, C62x, C64x, DM67x, ARM7, ARM9, 68K/Coldfire

## Professional experiences summary

### **Nestwave, 09/2015 - today (RT-SW Arch, Cloud SW Arch, Multi-Threading; Python, Java, C; DevOps)**

- ✓ **Co-founded Nestwave** and served as **Engineering Director** until its acquisition by NextNav in 10/2022
- ✓ Acted as **Cloud Software Architect** and Cloud Team Manager
  - **Created from scratch BE services, based on FastAPI framework.** Used **git submodule** to synchronize **multiple git repositories**
  - **Defined use case, communication, sequence and interaction diagrams.**
  - **Designed low latency cloud service architecture** using C-DLL/SO within Python code. **Ensured response time less than 100ms.**
  - **Led migration to AWS of cloud infrastructure based on Kubernetes, Terraform, Ingress, ALB, NLB, CloudFront, HA Proxy**
  - **Improved significantly work processes** by introducing CI/CD methodology, issues tracking, code review and unit testing
  - **Specified reusable SW components** implementing **machine learning models** to improve positioning and multi-path mitigation
- ✓ Acted as **Embedded Real Time Software Architect** and Firmware Team Manager
  - **Wrote system requirements, use case definitions, interfaces specification, user manual, test plan documents.**
  - **Defined layered FW architecture.** Produced **interaction overview, state machine and timing diagrams**
  - **Reduced by half MIPS & memory footprints** by giving hint on algorithms improvement to fit DSP architecture constrains
  - **Introduced DevOps automation tools, issues tracking, code review and unit testing. Improved significantly work processes**

### **NXP Semiconductors, 12/2013 - 08/2015 (RT-SW Arch, Multi-Tasking; Matlab, C)**

- ✓ **DSP FW architect** responsible of audio smart amplifiers for handsets and tablets
  - **Reworked architecture specifications** of SoC and DSP FW: **System requirements analysis**, MIPS budget estimation
  - **Revamped work process**, designed internal tools for **accelerating development and validation by a factor of 4**
- ✓ Successfully conducted process and **attained ISO9001 certification** and process improvement recognition

### **SEQUANS Communications, 08/2005 – 11/2013 (RT-SW Arch, Multi-Threading; Python, C, C++)**

- ✓ **Senior solution engineer managing** a 4G host application for **strategic big accounts**: program management, dev & plan tracking
- ✓ **Project manager** on WIMAX program, **overseeing SW releases** for middle priority customers
- ✓ **DSP μCode team leader** for the WIMAX and LTE PHY & MAC SoC projects
  - Led team and development. Produced **event driven architecture** and **HW-SW interfaces specifications**

### **ENERTEC, 07/2002 - 10/2004; ATMEL, 09/2001 - 07/2002 (RT-SW Arch, Multi-Tasking; C)**

- ✓ **Embedded real time software engineer** working on DSP and FPGA based aircraft signals recorder acquisition cards
- ✓ **DSP architecture junior engineer** contributing to design, performance analysis and test of a SIMD/VLIW DSP core

### **Open Source Community, since 1999 (SW Arch, Multi-Tasking; Pascal, C, Make)**

- ✓ Head of Free Pascal & Lazarus team in the Debian Project, packaging programs for multiple platforms
- ✓ Free Pascal Compiler and Lazarus IDE projects member (with commit rights): ported FPC to Sparc64, Fixed GTK3 bindings